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Table of Contents

Note : Remove “Table of Content” before including in CP Book

Each Course Plan shall be printed and made into a book with cover page
Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

15cs72C : Advanced computer Architecture

A. COURSE INFORMATION

1. Course Overview

Degree:	B E	Program:	CS&E
Year / Semester :	7	Academic Year:	2018-19
Course Title:	Advanced Computer Architecture	Course Code:	15cs72
Credit / L-T-P:	4/4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	52	SEE Marks:	80Marks
CIA Marks:	20	Assignment	1 / Module
Course Plan Author:	ASHA H R	Sign	Dt:30/7/2018
Checked By:		Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	Theory of Parallelism: Parallel Computer Models, The State of Computing, Multiprocessors and Multi-computer, Multivector and SIMD Computers ,PRAM and VLSI Models, Program and Network Properties ,Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.	10	Parallel Computer Models performance of Parallel Model	L2, L3
2	Processors and Memory Hierarchy, Advanced Processor Technology, Super scalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.	10	Processors and Memory Organization Processors and Memory Design	L2 ,L4
3	Bus, Cache, and Shared Memory ,Bus Systems ,Cache Memory Organizations ,Shared Memory Organizations ,Sequential and Weak Consistency Models ,Pipelining and Super scalar Techniques ,Linear Pipeline Processors ,Nonlinear Pipeline Processors ,Instruction Pipeline Design ,Arithmetic Pipeline Design	10	Bus and Cache Organization Bus and Cache Design	L2 ,L4
4	Multiprocessors and Multicomputers ,Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers ,Message-Passing Mechanisms ,Multivector and SIMD Computers ,Vector Processing Principles ,Multivector Multiprocessors ,Compound Vector Processing ,SIMD Computer Organizations. Scalable, Multi-threaded, and Data flow Architectures, Latency-Hiding Techniques, Principles of Multithreading, Fine-Grain Multicomputers, Scalable and Multithreaded Architectures, Data flow and Hybrid Architectures	10	Parallel Computer Architectures Scalable Computer Architectures	L3,L4
5	Software for parallel programming: Parallel Models, Languages, and Compiler ,Parallel Programming Models, Parallel Languages and Compilers ,Dependence Analysis of Data Arrays ,Parallel Program Development and Environments, Synchronization and Multiprocessing Modes. Instruction and System Level Parallelism, Instruction Level Parallelism ,Computer Architecture, Contents, Basic Design Issues ,Problem Definition ,Model of a Typical Processor ,Compiler-detected Instruction Level Parallelism ,Operand Forwarding ,Reorder Buffer, Register Renaming ,Tomasulo's Algorithm ,Branch Prediction, Limitations in Exploiting Instruction Level Parallelism ,Thread Level Parallelism.	10	Partitioning Parallel Programs for Multiprocessors Scheduling Parallel Programs for Multiprocessors	L2,L3
6				

3. Course Material

Module	Details	Available
1	Text books	
	Kai Hwang and Naresh Jotwani, Advanced Computer Architecture (SIE): Parallelism, Scalability, Programmability, McGraw Hill Education 3/e. 2015	In Lib
2	Reference books	
	John L. Hennessy and David A. Patterson, Computer Architecture: A quantitative approach, 5th edition, Morgan Kaufmann Elseveir, 2013	In dept
3	Others (Web, Video, Simulation, Notes etc.)	
	https://www.mhhe.com/hwang/aca3	Available

4. Course Prerequisites

S No	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	17cs34	Computer Organization	1.Knowledge of Processor performance	3	Conducted Seminars	L2,L3
	-	-	3.Concepts of Memory Organization	-		L2,L3
			5.Concepts of Multiprocessors			

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
15cs72 CO1	Understands the Parallel Computer Models	5	Parallel Computer Models	Demonstrate	Slip Test	L2 Understand
CO2	Calculate the Performance of Parallel Model	5	Performance of Parallel Computer	Problem solving	illustrate	L3 Apply
CO3	Understands the Organization of Processors and Memory	5	Organization of Processors and Memory	Demonstrate	Q&A	L2 Understand
CO4	Design of Processors and Memory	06	Processors and Memory Design	Examine	Differentiate	L4 Analyse
CO5	Understands the Organization of Bus and Cache	05	Organization of Bus and Cache	Demonstrate	Think-Pair - Share	L2 Understand
CO6	Analyzes the design of superscalar pipelining	05	Superscalar pipelining	Analyze	Questions	L4 Analyse
CO7	Design the different types of computer	06	Design of Computer	Practice in Multiple Contexts	Self-evaluation	L3 Apply
CO8	Analyses the Scalable Architecture	04	Scalable Architecture	Discussion	Student Presentation	L4 Analyse
CO9	Understands the Parallel Models,Languages and compilers	06	Languages and compilers	Demonstrate	Think-Pair - Share	L2 Understand
CO10	Develops the parallel programming environments	05	parallel programming	Develop	Self-evaluation	L3 Apply
-	**Total**	**52**	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	Numeric weather forecasting	CO1	L3
2	Oceanography and Astro physics	CO2	L4
3	Socio economics	CO3	L3
4	Fine Element analysis	CO4	L4
5	Artificial Intelligence and Exploration	CO5	L3
6	Genetic Engineering	CO6	L4
7	Weapons Research and Defense	CO7	L3, L5
8	Remote Sensing Applications	CO8	L3
9	Medical applications	CO9	L3
10	Energy Resource Exploration	CO10	L3

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes														
#	COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	Teach. Hours	Level
15CS72.1	Understands the Parallel Computer Models		1	1	1							1	1	1	1	5	L2
15CS72..2	Calculate the Performance of Parallel Model	2	2	2		2				2	2	2			2	5	L3
15CS72.3	Understands the Organization of Processors and Memory	1	1	1	1			1					1	1		5	L2
15CS72.4	Design of Processors and Memory	2	2	2	2	2						2	2		2	06	L4
15CS72.5	Understands the Organization of Bus and Cache	1	1		1			1			1		1	1		05	L2
15CS72.6	Analyzes the design of superscalar pipelining	2	2	2	2					2	2		2		2	05	L4
15CS72.7	Design the different types of computer	2	2	2	2							2	2		2	06	L3
15CS72.8	Analyses the Scalable Architecture	2	2		2					2	2		2			04	L4
15CS72.9	Understands the Parallel Models,Languages and compilers	1	1	1	1								1	1		06	L2
15CS72.10	Develops the parallel programming environments	2	2	2	2							2	2		2	05	L3
	levelAVG	**1.7**	**1.6**	1.6	1.6	**2**		**1**		**3**	1.8	**1.8**	**1.6**	**0.8**	**1.8**		
	Hours avg															**5.2**	

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**		

Dept
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CO1	PO2	The students will analyze the basic concepts of different parallel computer architecture		L2

CO1	PO3	Designed different flow mechanism for partitioning of parallel program	L3
CO1	PO4	The knowledge of basic concepts of processes will help the students to apply the same to formulate solutions for engineering problems	L3
CO1	PO7		
CO1	PO11		
CO1	PO12	Study of Parallel Computer architecture is required if students want to work in system as well as companies.	
CO2	PO1	The knowledge of basic formulate solutions for engineering problems are applied to calculate the Performance of Parallel Models	L2
	PO2	Analyze how parallel processing has become frontier challenge in super computer application	
CO2	PO3		
CO2	PO5		L4
CO2	PO9		
CO2	PO10		
CO2	PO11		
CO2	PO9	Functions effectively as an individual and as member of team work is necessary to analyze workload,resources of parallel computer effective analysis	L3
CO3	PO1	Students should have the knowledge of different processor and memory architecture and how is the representation of RISC AND CICS processors	L2
CO3	PO12		
CO3	PO2	Students should analyze how data is sent to different architecture and how we perform different operations and how the storage of data is done	L4
CO3	PO3		
CO3	PO4		
CO3	PO7		
CO4	PO2	Analyze the different architecture of processor and memory architecture	L4
CO4	PO1		
CO4	PO4		
CO4	PO3	Develop efficient processor and memory architecture which will translate sequential programs to machine language and contain some instruction level parallelism	L6
CO4	PO11	Conduct some investigation of page faults,hits ratios and memory replacement in RISC ,CICS ,Supercomputers and in VLIW architectures	L4
CO4	P12		
CO5	PO1	Apply the knowledge of buses,system interfaces and slot connections to various function boards in multiprocessor system	L3
CO5	PO	Analyze the Bus addressing,timing protocols and interrupt	L4
CO6	PO2	Analyze the speedup,efficiency and throughput of different pipelining processors	L4
CO5	PO7		
CO5	PO10		
CO5	PO12		
CO6	PO10		
CO6	PO3	Design the state transition diagrams for pipeline	L6
CO6	PO9	Conduct pipelining operations as team work using hardware score board	L3

CO6	PO1		
CO6	PO2		
CO6	PO4		
CO6	PO12		
CO7	PO1	Apply the knowledge of modern tools ,multiprocessors and multicomputers	L3
CO7	PO2	Analyze how multiprocessor systems are interconnected ,multistage network and input output levels	L4
CO7	PO3	Students will design multicast routing algorithms	L6
CO7	PO4		
CO7	PO12		
CO7	PO11		
CO8	PO1	Apply the knowledge of multiprocessor and multicomputers	L3
CO8	PO2	Analyze the multi-threading issues and solutions	L4
CO8	PO9	Team work is needed to analyses the network memory structure and data flow in computers	L4
CO8	PO4		
CO8	PO10		
CO8	PO12		
CO9	PO1	Students should have the knowledge of parallel programing Models and compilers	L2
CO9	PO4	Different geometric view of SIV,ZIV tests are conducted for parallel compilers and analyses different matrix	L4
CO9	PO2		
CO9	PO3		
CO9	PO4		
CO9	PO12		
CO9	PO10		
CO10	PO2	Analyze different dependences and different protocol monitors	L4
CO10	PO3	Design different tools and hardware platforms for computing models	L4
CO10	PO1		
CO10	PO4		
CO10	PO11		
CO10	PO12		
CO10	PO7	Simulation is used to measure the effects of scheduling weather	L5

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Module #	Title	Teaching Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		

Dept
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1	Parallel Computer Models	11	2	-	-	1	1	2	CO1, CO2	L2, L3
2	Hardware Technologies:	10	2	-	-	1	1	2	CO3, CO4	L2, L4
3	Bus, Cache, and Shared Memory	10	-	2	-	1	1	2	CO5, CO6	L2, L4
4	Parallel and Scalable Architectures	11	-	2	-	1	1	2	CO7, C08	L3,L4
5	Software for parallel programming: Models	10	-	-	4	1	1	2	CO9, CO10	L2, L3
-	**Total**	**52**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	15	CO1, CO2, CO3, CO4	L2, L3,L2,L4
CIA Exam – 2	15	CO5, CO6, CO7, C08	L2, L4, L3, L4
CIA Exam – 3	15	CO9, CO10	L2, L3
Assignment - 1	05	CO1, CO2, CO3, CO4	L2, L3,L2,L4
Assignment - 2	05	CO5, CO6, CO7, CO8	L2, L4, L3, L4
Assignment - 3	05	CO9, CO10	L2, L3
Seminar - 1	-	-	-
Seminar - 2	-	-	-
Seminar - 3	-	-	-
Other Activities – define – Slip test			
Final CIA Marks	**20**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN - 1

Module - 1

Title:	Parallel Computer Models	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-		-	**Level**
1	Understands the concept of Parallel Computer Models	CO1	L2
2	Calculate the Performance of Parallel Model	CO2	L3
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction to Parallel Computer Models	C01	L2
2	Classes of computers	C01	L2
3	Defining Computer Architectures	C01	L2
4	Trends in Technology	C01	L2
5	Trends in Power Integrated Circuits	C01	L2
6	Multivector and SIMD Computers	C01	L2
7	PRAM and VLSI Models	C01	L2
8	Program Partitioning and Scheduling	CO2	L3
9	Program Flow Mechanisms	CO2	L3
10	Principles of Scalable Performance	CO2	L3
11	System Interconnect Architectures	CO2	L3
12	Performance Metrics and Measures	CO2	L3
13	Parallel Processing Applications	CO2	L3
14	Speedup Performance Laws	CO2	L3
15	Scalability Analysis and Approaches	CO2	L3
c	**Application Areas**	**CO**	**Level**
1	Numeric weather prediction	CO1	L2
2	Oceanography and Astrophysics	CO2	L3
d	**Review Questions**	-	-
1	Explain Computer Architectures ?	CO1	L2
2	Explain Five generations of Electronic Computers ?	CO1	L2
3	Explain SIMD and Multi vector Computers ?	CO2	L2
4	Explain Program Flow Mechanism ?	CO2	L3
5	Find the number of dies per 300mm water for a die that is 1.5 cm on a side	CO2	L3
e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module – 2

Title:	Divide and Conquer	Appr Time:	10 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Organize and design the Processors	CO3	L2
2	Organize and design the Memory	CO4	L4
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
17	Hardware Technologies,,,,	CO3	L2
18	Processors and Memory Hierarchy	CO3	L2
19	Super scalar and Vector Processors	CO3	L2
20	Advanced Processor Technology	CO3	L2
21	Memory Hierarchy Technology	CO3	L2
22	Virtual Memory Technology.	CO4	L4
23	Cache performance	CO4	L4
24	Six basic cache Optimizations	CO4	L4
25	Protection and examples of Virtual Memory	CO4	L4
c	**Application Areas**	**CO**	**Level**
1	Use in smart phones	CO3	L2
2	Used in Database system Implementation	CO4	L4
d	**Review Questions**	-	-
12	What are the different hardware technologies ?	CO3	L2
13	Explain Memory Hierarchy with neat diagram ?	CO3	L2
14	Explain different advanced technologies and Superscalar operation ?	CO3	L2
15	Explain Vector Processors & Virtual Memory Technology?	CO4	L4
16	Explain Scalar Processor with neat diagram ?	CO4	L4
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code: 15CS72 Sem: 7 Marks: 30 Time: 75 minutes
Course: Advanced computer Architecture

-	-	**Note: Answer any 3 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Define the following terms : i) Computer Architecture ii) Learning curve iii) Response time iv) Throughput.	15	CO1	L2
	b	Define Amdahl's law. Derive an expression for CPU clock as a function of instruction count, clock per instruction and clock cycle time.		CO1	L2
	c	Find the die yield for dies that are 1.5cm on a side and 1.0cm on a side, assuming a defect density of 0.4 per cm2 and is 4.		CO2	L3
	d	Explain the main measures of dependability.		CO2	L3
2	a	Explain how the protection of processes is accomplished via the following : i) Virtual memory ii) Virtual machines.	15	CO1	L2
	b	What do you understand by memory consistently? Explain furthermore, discuss how relaxed consistently models allow reads and write to complete out of order.		CO1	L2
3	a	rite note on the performance equation of processor.	15	CO4	L4
	b	Assume a disk subsystem with the following components and MTTF. • 10 disks each rated at 1.000,000 hr MTTF • 1 SCSI controller, 500,000 - hour MTTF • 1 Power supply, 200,000 , - hour MTTF • 1 Fan, 200, 000 — hour MTTF. • 1 SCSI cable, 1,000,000 — hour. Using the simplifying assumptions that the lifetimes are exponentially distributed and that failure are independent, compute the MTTF of the system as a whole.		CO4	L4
4	a	Explain any four memory hierarchy questions in detail.	15	CO3	L2
	b	Explain the different techniques used to improve memory performance inside a DRAM chip.		CO3	L2

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code: 15CS72 Sem: 7 Marks: 5 / 10 Time: 90 – 120 minutes

Course: Advanced computer Architecture

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain the State of Computing ?	5	CO1	L2
2		Explain the Evolution of Computer Architecture ?	5	CO1	L3
3		Explain Two NUMA models of Multiprocessor system ?		CO2	L3
4		Explain System Interconnect Architectures ?	5	CO1	L2
5		Explain Static and Dynamic Connection Networks ?	5	CO2	L2
6		Briefly explain Advanced Processor Technology ?	10	CO1	L3
7		Explain Intel i860 processor architecture ?	10	CO1	L3
8		Explain Vector and Symbolic Processor ?	10	CO2	L3
9		Define the characteristics of Symbolic Processing ?	10	CO2	L2
10		Explain Memory Hierarchy ?	10	CO2	L3

D2. TEACHING PLAN - 2

Module – 3

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the Organization of Bus and Cache	CO5	L2
2	Design the bus and Cache	CO6	L4

b ***Course Schedule***

Class No	Module Content Covered	CO	Level
1	Bus, Cache, and Shared Memory ,,Shared Memory Organizations ,Sequential and ,,Linear Pipeline Processors ,Nonlinear Pipeline Processors ,Instruction Pipeline Design ,Arithmetic Pipeline Design	CO5	L2
2	Bus, Cache, and Shared Memory ,Bus Systems	CO5	L2
3	Bus Systems ,Cache Memory Organizations	CO5	L2
4	Pipelining and Super scalar Techniques	CO5	L2
5	Weak Consistency Models	CO5	L2
6	Cache Memory Organizations ,,	CO6	L4
7	Shared Memory Organizations	CO6	L4
8	Sequential and Weak Consistency Models ,,	CO6	L4
9	Pipelining and Super scalar Techniques	CO6	L4
10	Linear Pipeline Processors ,Nonlinear Pipeline Processors ,	CO6	L4
11	Instruction Pipeline Design ,Arithmetic Pipeline Design	CO6	L4

c	**Application Areas**	**CO**	**Level**
1	Use to find performance of processors	CO5	L2
2	Used in Memory Organization	CO6	L4

d	**Review Questions**	-	-
1	What is Shared Memory organization explain ?	CO5	L2
2	Explain ,Cache Memory Organizations?	CO5	L2
3	Compare Sequential and Weak Consistency Models?	CO6	L4
4	Write a short note on Pipelining and Superscalar Techniques?	CO6	L4
5	Explain Arithmetic Pipeline Design with diagram ?	CO6	L4

e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module – 4

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
1	Used to analyze Multiprocessors and Multicomputers ,Multiprocessor System	-	**Level**
2	Used to design Scalable Architectures	CO7	L3
b	***Course Schedule***	CO8	L4
Class No	**Module Content Covered**	**CO**	**Level**
1	Parallel Multiprocessors and Multicomputers ,Multiprocessor System	CO7	L3
2	Cache Coherence and Synchronization Mechanisms	CO7	L3
3	Three Generations of Multicomputers	CO7	L3
4	Message-Passing Mechanisms	CO7	L3
5	Multivector and SIMD Computers	CO7	L3
6	Vector Processing Principles	CO7	L3
7	Multivector Multiprocessors	CO7	L3
8	Compound Vector Processing	CO7	L4
9	SIMD Computer Organizations. Scalable	CO8	L4
10	Multi-threaded, and Data flow Architectures	CO8	L4
11	Principles of Multithreading	CO8	L4
12	Fine Grain Multicomputers	CO8	L4
13	Scalable and Multithreaded Architectures	CO8	L4

c	**Application Areas**	**CO**	**Level**
1	Use to determine different Platformas	CO7	L3
2	Used in networks	CO8	L4
d	**Review Questions**	-	-
1	Difference between Multiprocessors and Multi computers ?	CO7	L3
2	What is Cache Coherence and explain ?	CO7	L3
3	What is Compound Vector Processing and explain ?	CO8	L4
4	Explain Multithreaded, and Dataflow Architectures ?	CO7	L3
5	Explain different Multithreading techniques ?	CO8	L4
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code: 15CS72 Sem: 7 Marks: 30 Time: 75 minutes
Course: Advanced computer Architecture

		Note: Answer any 2 questions, each carry equal marks.	**Marks**	**CO**	**Level**
1	a	Which are the major categories of advanced optimizations of cache performance? Explain any one in detail.	15	CO5	L3
	b	Explain DRAM memory technology with its basic organization.		CO5	L3
2	a	Explain the .basic VLIW approach for exploiting ILP, using multiple issues.	15	CO6	L4
	b	Explain branch target buffer with neat diagram.		CO6	L4
	c	.What are the issues involved in implementation of speculation? Explain register renaming approach.		CO6	L4
3	a	With appropriate timing diagrams, explain the concept of delayed branch technique used in RISC processors. What are its limitations and demonstrate the scheduling of branch delay with suitable examples.	15	CO7	L3
	b	Explain what is branch penalty? Discuss the different techniques used to reduce branch penalties.		CO7	L3
	c	Consider a non-pipelined processor in RISC. Assume that it has ins clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and set up, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speed up in the instruction execution rate is achieved from this pipeline?		CO7	L3
4	a	Explain the steps to unroll the code and schedule.	15	CO8	L4
	b	What is the drawback of 1 — bit dynamic branch prediction method? Clearly state, how to overcome in 2 — bit prediction. Give the state transition diagram of 2 — bit predictor.		CO8	L4

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code: 15CS72 Sem: 7 Marks: 5 / 10 Time: 90 – 120 minutes
Course: Advanced computer Architecture
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain the Hierarchical Bus system ? Explain the Cache Coherence and Synchonization Mechanism	5	CO8	L4
2		Explain three generation of Multicomputers ?	5	CO7	L3
3		Explain the Vector and Scalar performance of various Supercomputers ?		CO7	L3
4		What is Cray/MPP system ? Explain	5	CO7	L3
5		Explain Shared Virtual Memory ?	10	CO8	L4
6		Explain the Multidimensional Architectures ?	10	CO8	L4
7		What is MIT J-machine ? Explain	10	CO8	L4
8		Explain Instruction Set Architecture ?	10	CO8	L4
9		Explain Tera Multiprocessor system	10	CO7	L3
10		Explain the Data Flow Architectures ?	10	CO7	L3
11					

D3. TEACHING PLAN - 3

Module – 5

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understands Instruction Level Parallelism	CO9	L2
2	Analysis of Data Arrays	CO10	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Parallel Models, Languages, and Compiler	CO9	L2
2	Dependence Analysis of Data Arrays	CO9	L2
3	Parallel Program Development and Environments	CO9	L2
4	Synchronization and Multiprocessing Modes.	CO9	L2
5	Instruction and System Level Parallelism	CO9	L2
6	Instruction Level Parallelism	CO9	L2
7	Computer Architecture ,Contents,Basic Design Issues	CO9	L2
8	Problem Definition	CO10	L3
9	Model of a Typical Processor	CO10	L3
10	Compiler-detected Instruction Level Parallelism	CO10	L3
11	Operand Forwarding	CO10	L3
12	Reorder Buffer, Register Renaming		
13	Tomasulo's Algorithm Branch Prediction		
14	Limitations in Exploiting Instruction Level Parallelism		
15	Thread Level Parallelism.		
c	**Application Areas**	**CO**	**Level**
1	Use to find performance of algorithm	CO10	L3
2	Used in Searching and sorting	CO9	L2
d	**Review Questions**	-	-
1	Explain different Languages, and Compilers for parallel programming ?	CO9	L2
2	Explain Parallel Program Development and Environments?	CO9	L2
3	Explain Instruction and System Level Parallelism ?	CO10	L3
4	Write a short note on Register Renaming ,Tomasulo's Algorithm?	CO10	L3
5	How to Exploit Instruction Level Parallelism and Thread Level Parallelism?	CO10	L3
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code: 15CS72 Sem: 7 Marks: 30 Time: 75 minutes

Course: Advanced computer Architecture

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	What makes pipelining hard to implement?	15	CO9	L2
	b	Explain in detail, the hardware support for preserving exception behavior during speculation		CO9	L2
2	a	Explain the architecture of IA64 intel processor and also prediction and speculation support provide	15	CO9	L2
	b	Discuss how software pipelining and trance, scheduling techniques are useful in uncovering the parallelism among instructions by creating longer sequences of straight sine code.		CO9	L2
	c	Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram.		CO9	L2
3	a	With a neat diagram. explain the translation buffer of fast address translation.	15	CO 10	L3
	b	Explain the internal organization of 64M bit DRAM.		CO 10	L3
4	a	What is instruction level parallelism? Explain control dependence using code fragment	15	CO 10	L3
	b	Explain storage structure of superscalar computers		CO 10	L3

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code: 15CS72 Sem: 7 Marks: 5 / 10 Time: 90 – 120 minutes

Course: Advanced computer Architecture

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		What is poison bit ? Explain the methods for preserving exception behavior?	10	CO9	L2
2		How is multi threading used to exploit thread level parallelism within a processor? Multi threading – definition Fine grained multi threading Coarse grained multi threading Simultaneous multi threading	10	CO9	L2
3		Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram.	10	CO10	L3
4		Explain Dependence Analysis of Data Arrays ?	10	CO10	L3
5		Explain Parallel Languages and Compilers ?	10	CO10	L3

F. EXAM PREPARATION

1. University Model Question Paper

Course: Advanced computer Architecture — Month / Year: May /2018
Crs Code: 15CS72 — Sem: 7 — Marks: 80 — Time: 180 minutes

		Note Answer all FIVE full questions. All questions carry equal marks.	**Marks**	**CO**	**Level**
1	a	What do you mean by instruction set Architecture (ISA)? Briefly explain the various dimensions of ISA addressed during defining the computer architecture.	16 / 20	CO1	L2
-	b	Explain Five generations of Electronic Computers ?	16 / 20		
	a	Explain the main measures of dependability.		CO2	L3
	b	Write note on the performance equation of processor.			
2	a	Explain the Multidimensional Architectures ?	16 / 20	C03	L2
	b	Explain in detail the hardware support for preserving exception behaviour during speculation		C03	L2
	c	What is Cray/MPP system ? Explain		C04	L4
-	a	What is MIT J-machine ? Explain	16 / 20	C04	L4
	b	Explain Shared Virtual Memory ?		C04	L4
3	a	Indicate the distinguish features of the following techniques employed to improve cache behavior. i) Compulsory misses ii) Capacity misses (iii) Conflict misses (05 Marks) c. In brief, discuss the four memory hierarchy questions for virtual memo	16 / 20	CO5	
	b	snooping with respect to cache — coherence protocol.			
	c				
	d				
-	a	With a neat diagram, explain the hypothetical memory hierarchy	16 / 20	CO5	
	b	Explain the Data Flow Architectures ?		CO7	L3
4	a	Explain the Multidimensional Architectures ?	16 / 20	CO7	L3
	b	What is MIT J-machine ? Explain			
-	a	What is prefetching in SVM ? how it is done ?	16 / 20	CO8	L4
	b	Explain Latency problems for remote loads and local loads ?		CO8	L4
5	a	What is poison bit ? Explain the methods for preserving exception behavior?	16 / 20	CO9	L2
	b	Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram.		CO10	L3

a	What do you mean by forward and backward approach of problem solving in Dynamic programming?		CO10	L3
b	Analyze precisely the computing time and space requirements of this new version of Prim's algorithm using adjacency lists.		CO10	L3

2. SEE Important Questions

Course: Advanced computer Architecture — Month / Year May /2018
Crs Code: 15CS72 Sem: 7 Marks: 80 Time: 180 minutes
Note Answer all FIVE full questions. All questions carry equal marks.

Module	Qno.	Important Question	Marks	CO	Year
1	1	Explain different classess of Computer . Illustrate the seven dimensions of an ISA	16 / 20		2015
	2	Explain different trends in Integrated Circuits			2004
	3	Give a brief explanation about trends in power in integrated circuits and cost			2014
	4	How response time, execution time and throughput are interrelated with each other			2007
	5	Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side assuming a defect density of 0.4 per cm2 and a is 4. Define Amdahl's law. Derive an expression for cpu clock as a function of instruction count. Clocks per instruction and clock cycle time.			2015
2	1	Explain how the protection of processes is accompolisbed via the following : i) Virtual memory ii) Virtual machines.	16 / 20		2005
	2	Explain the process of protecting via virtual Memory			2015
	3	Explain hardware support for exposing parallelism for VLIW & EPIC			2017
	4	Explain in detail the hardware support for preserving exception behavior during speculation			2006
	5	Write short notes on : i) The Itanium 2 processor ii) IA -64 register model			2004
3	1	Explain AMD opteron Memory Hierarchy	16 / 20		2006
	2	Explain in detail, Branch —Target buffers			2015
	3	snooping with respect to cache — coherence protocol.			2007
	4	Explain in detail, the architecture support for protecting processes from each other via virtual memory			2014
	5	Explain the six basic cache optimization techniques.			2017
4	1	Explain the different taxonomy of parallel architecture.	16 / 20		2014
	2	With neat diagram explain the basic structure of a central' shared memory and distributed shared memory multiprocessor			2014/ 17
	3	With a neat diagram, explain the basic structure of a centralized shared memory and distributed memory multiprocessor.			2006
	4	Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential?			2017
	5	Explain basic schemes for enforcing coherence.			2017
5	1	Explain the basic Compiler techniques for exploring Instruction-Level Parallelism	16 / 20		2009
	2	Explain exploiting ILP using dynamic scheduling multiple issue and speculation.			2015
	3	Enlist the pipeline hazards. Also explain them.			2007

4	With an aid of a neat functional diagram, discuss the classic 5-stage pipeline for a Risc processor, that highlight how an instruction flows through the data path.	2018
5	Explain the design issues of parallel Computer	2005